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The Sight & Sound of Information

PLL Building Blocks

Presented by:
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Phased-Locked Loop Building Blocks

- Basic PLL Operation
- VCO
- Dividers
  - R Counter Divider
    - Relation to Crystal Reference Frequency
    - Relation to Comparison Frequency
  - N Counter Divider
    - Prescalers
    - Legal Divide Ratios
  - Programming Divider Ratios into a PLL
- Phase-Frequency Detector
- Charge Pump
- Loop Filter

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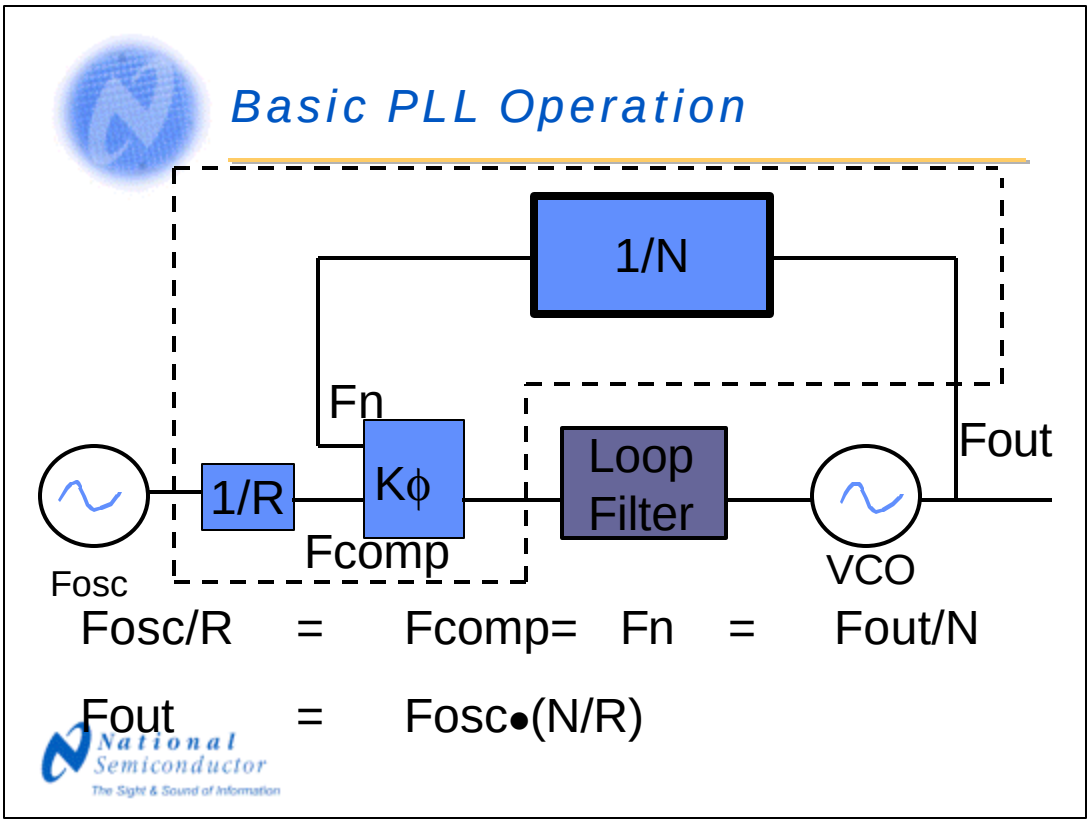
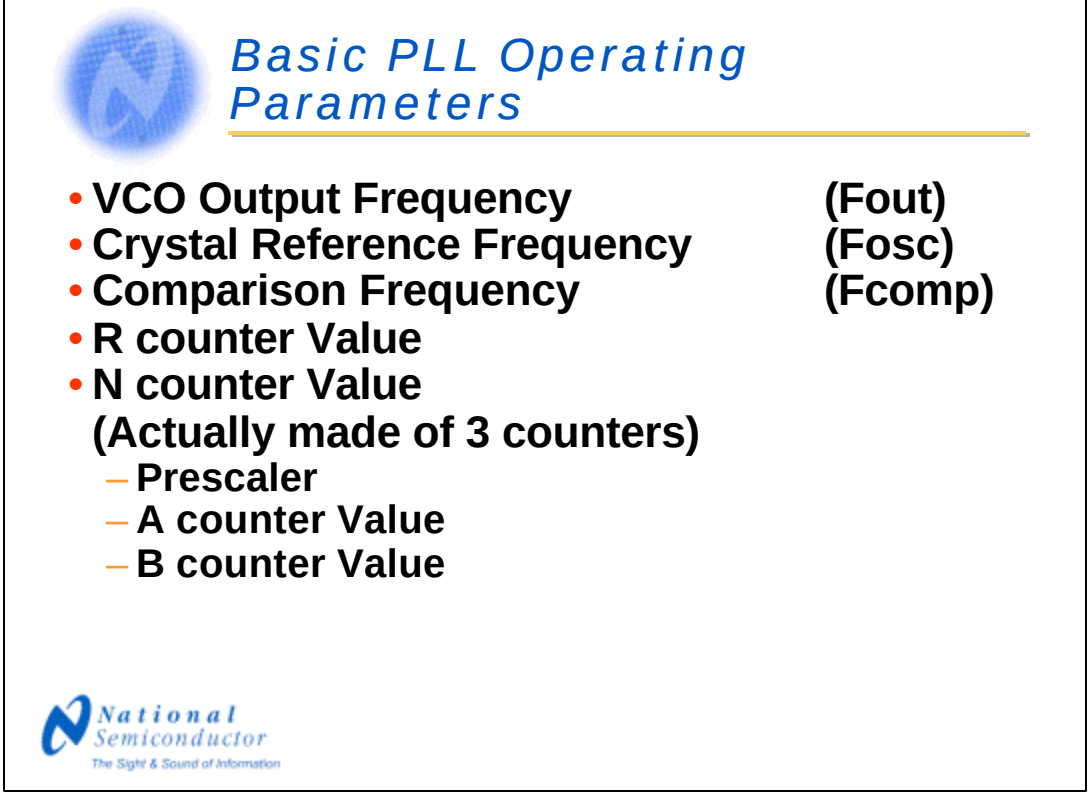


The way that the PLL works is a follows. There is a fixed crystal frequency (Fosc), which is divided down to the comparison frequency, Fcomp. Now the phase detector compares this signal to Fn. If the signals are the same, it puts out only very small corrections. If Fn>Fcomp, it sinks current. If Fn>Fcomp, it sources current. The loop filter is a low pass filter that converts these current corrections into a voltage. The VCO converts this voltage to a frequency. This output frequency, Fout is divided down by the N counter and compared to Fcomp. So the PLL basically steers the voltage to the VCO such that Fn = Fcomp.

The reason that the VCO can not be simply driven by a DAC is that VCOs have wide process variations and the output frequency can not be accurately determined by the input voltage. Typically, the crystal frequency (Fosc) is very stable, but is limited to much lower frequencies. The PLL also provides the very important advantage that the N counter can be changed by programming it to different values. This allows the PLL to be able to synthesize many different frequencies from a fixed frequency.



VCO Output Frequency (Fout)

This is the output of the whole system, which is controlled by the PLL

Crystal Reference Frequency (Fosc)

This is a fixed frequency. It can be provided by a TCXO (Temperature Compensated Crystal Oscillator) or a crystal. The crystal oscillator consists of a resonant circuit in the feedback path of an inverter. On some of National's PLLs, an inverter is included for using a crystal. Note that the difference between a crystal and crystal oscillator is that the crystal oscillator includes the inverter.

Comparison Frequency (Fcomp)

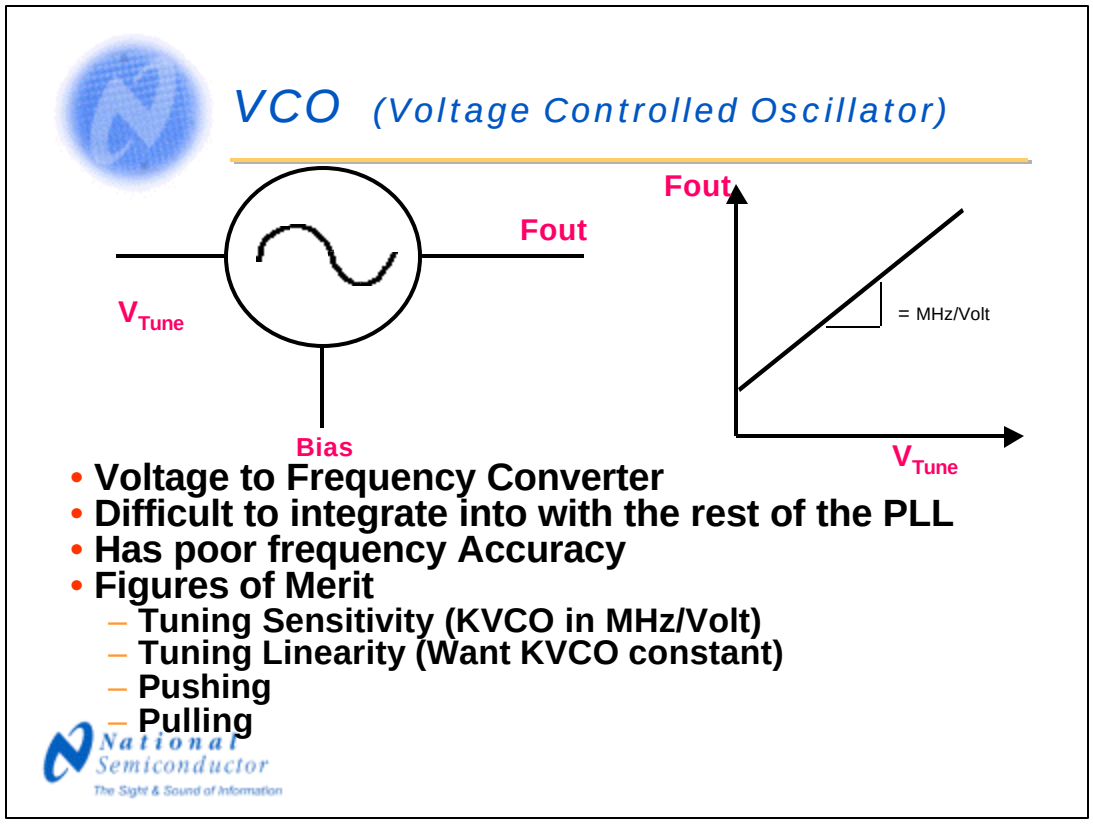
This can be thought of as the tuning resolution. As N is changed by 1, the output changes in increments of fcomp. For this reason, it is sometimes referred to as the channel spacing, although that name is not accurate, because there are a few isolated cases where it is something other than the channel spacing (Fractional N).

R Counter Value

This divides the fixed crystal reference frequency by R to get the comparison frequency. R is usually fixed for a given application.

N Counter Value

This multiplies the comparison frequency in order to get the output frequency. Note that the output frequency is tuned by changing the N counter value. The N counter actually consists of smaller counters in order to allow high frequency operation.



VCO Terminology

Tuning Sensitivity, Modulation Sensitivity, or KVCO

This is how much the output frequency changes for a given change in the voltage.

Tuning Linearity

Although design equations assume that the VCO gain is linear within some range, it typically has some nonlinear characteristics.

Usually, the tuning sensitivity is less at the higher tuning voltages.

Pulling

This is a drift in the output frequency caused by loading the VCO.

Load Pushing

A drift in the output frequency caused by changing the power supply voltage. One way to express this is in MHz/volt. It also gives an indication of how vulnerable the VCO is to power supply noise.

Other comments

The VCO contributes noise to the system. This is mostly outside the loop bandwidth.

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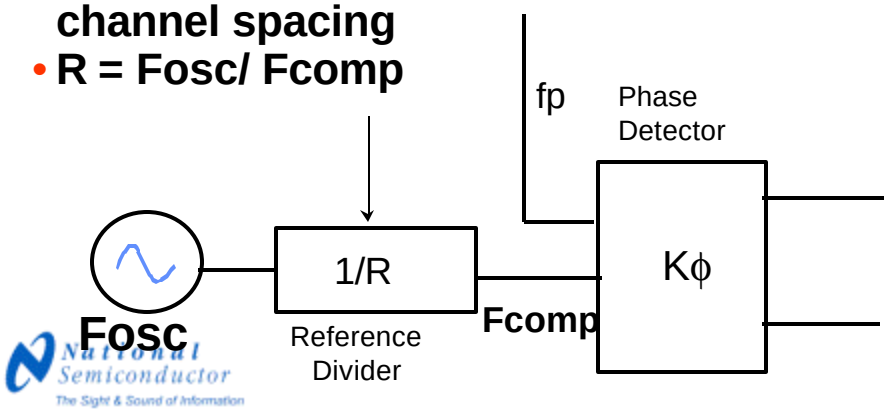
Crystal Reference, R counter, and Comparison Frequency

- **Crystal Reference is a crystal or TCXO at a fixed frequency. Frequency is Fosc.**
- **Comparison Frequency is the "tuning increment" which is typically equal to the channel spacing**
- **R = Fosc/ Fcomp**



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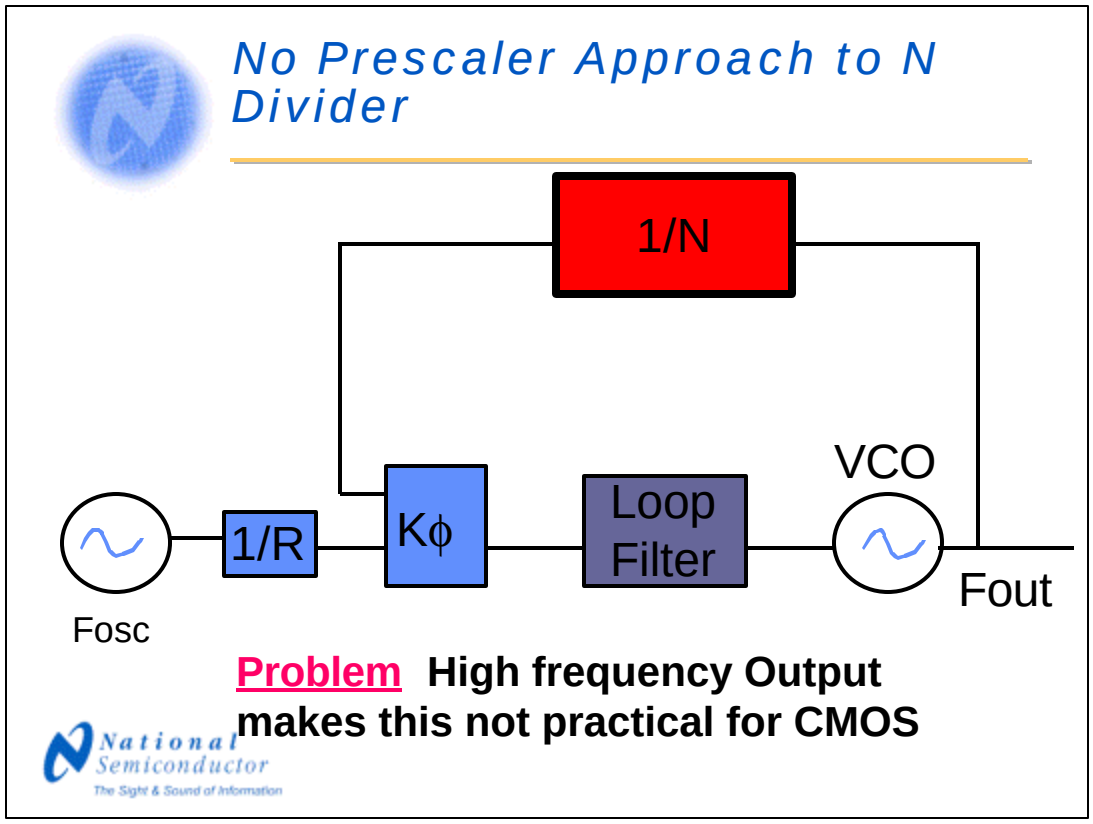
To determine what value should be programmed into the R counter, the comparison frequency must be known first. The comparison frequency is often chosen equal to the channel spacing since when N is changed by 1, the output frequency is changed by 1*Fcomp. Choosing the comparison frequency larger than this would cause the PLL to skip over channels, so this can not be done. The comparison frequency could be chosen smaller, but this would result in worse phase noise and a slower lock time -- the performance would not be as good. The restriction that the comparison frequency can not be chosen larger than the channel spacing applies only to integer N PLLs, not fractional N PLLs.

The crystal reference must be chosen so that is an integer multiple of the comparison frequency. Since Fcomp = Fosc / R, the value from the R counter can be easily determined.

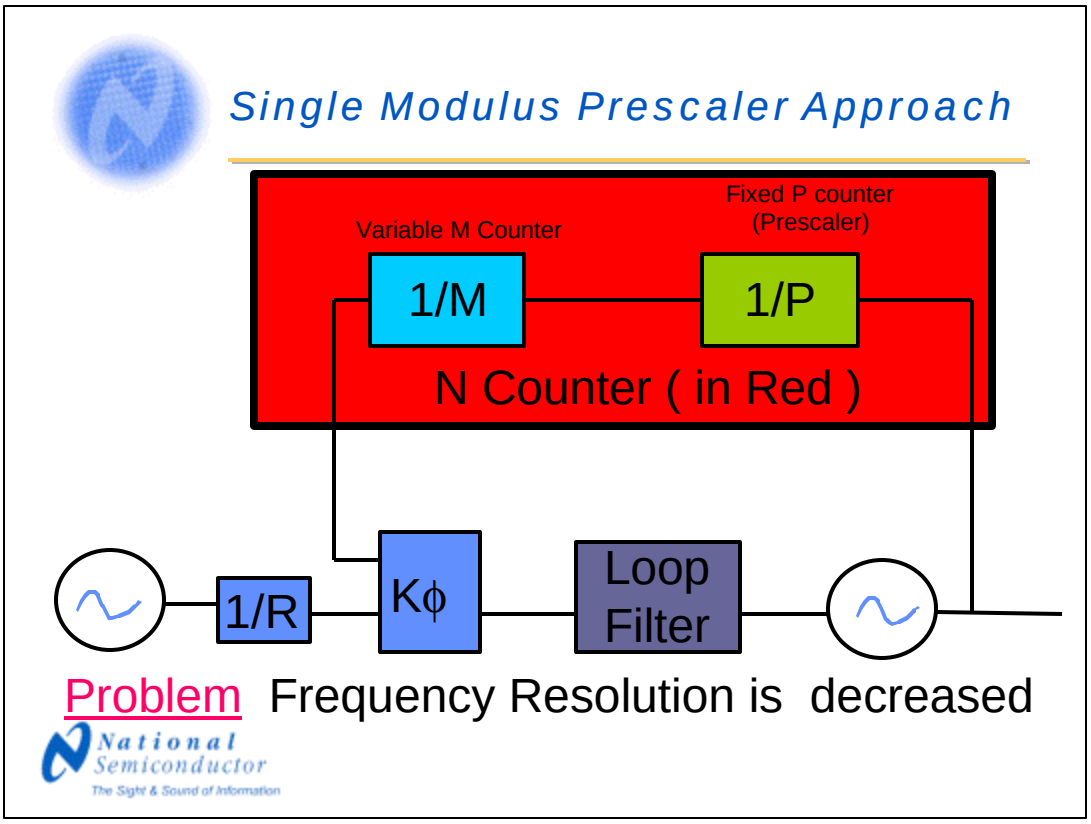


N Value Calculation

N is simply the output frequency divided by the comparison frequency.

Problem with Using a Simple Counter for the N Counter

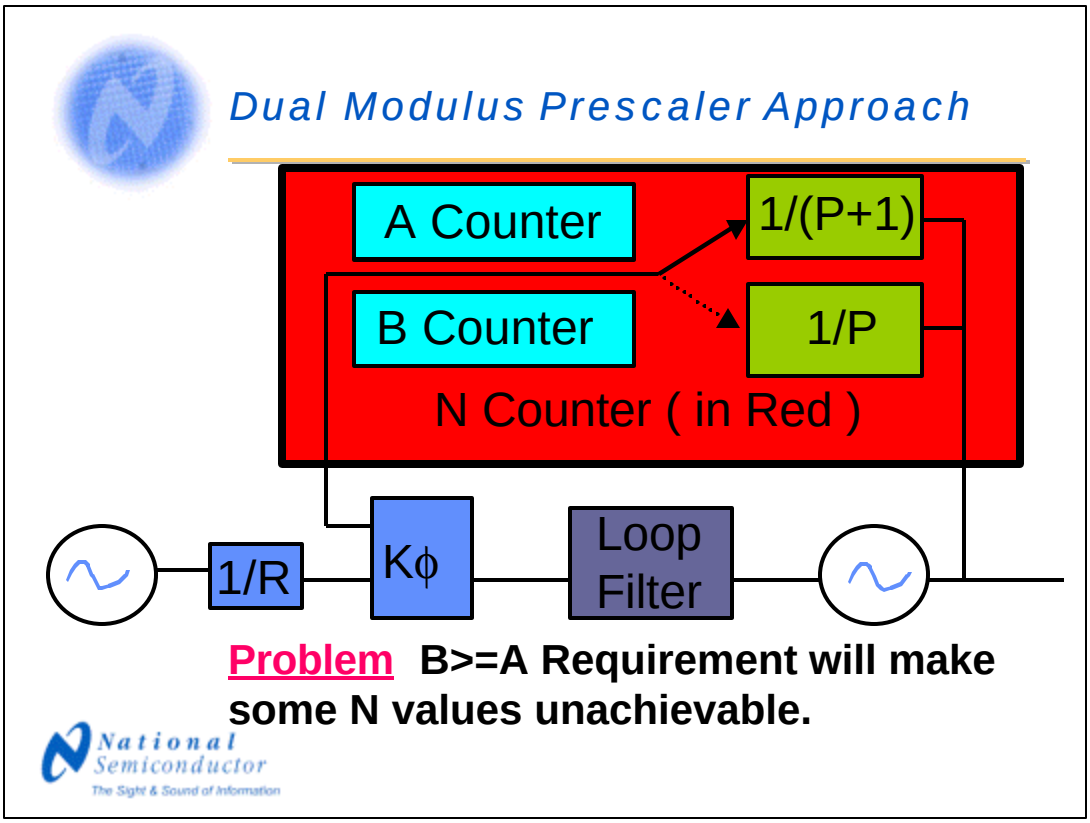
However, since the output frequency is typically high frequency, it is not practical to build it as a single counter because the high frequency process is good for the high frequency signal, but not so good for the rest of the functions on the PLL. This is why this is not used, except for low frequency.



Single Modulus Prescaler

This gets around the high frequency problem but sacrifices tuning resolution. This is why the Dual Modulus Prescaler (Next Slide) is typically used.

It is possible to reduce the comparison frequency by a factor of P, but this results in higher noise, and higher reference spurs.



Dual Modulus Prescaler Operation

1. Initially, the size P+1 prescaler is used.
2. Every P+1 cycles of the VCO, both the A and the B counters are decreased by 1.
3. This is continued until A=0. This takes a total of A*(P+ 1) VCO cycles.
4. Now the size P prescaler is switched in. Every P VCO cycles, The B counter is decreased by 1. Since the B counter was previously counting, this takes (B-A)*P VCO cycles.
5. When the B counter reaches 0, 1 pulse is given to the fp signal. This results in making N=A*(P+1)+(B-A)*P = P*B+A. Note also that this implies B>=A for proper operation

Dual Modulus Prescaler Operation

- In the previous slide, the size P+1 prescaler is first used, until the A counter reaches 0
  - This takes a total of A•(P + 1) counts
  - The B counter is simultaneously counting down
- The size P Prescaler is then switched in
  - The B counter starts with (B - A) counts
  - This takes (B - A)•P counts. This implies for proper operation that B>=A
- Adding the total counts gives the relationships
  - N = P•B + A
  - B = N div P, A = N mod P

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Determining The N Counter Value

- **P = Prescaler setting**
- **N = Fosc / Fcomp**
- **A requirement for proper operation of the PLL is B>=A**
  - **B = N div P**
  - **A = N - (B • P) = N mod P (Note A < P)**
  - **N = A(P+1) + (B-A)P = PB + A**
  - **Minimum Continuous Divide Ratio**
    - **If N >= P •(P-1) this guarantees B>=A**
    - **This does not mean N>=P •(P+1) is a necessary condition.**
  - **Note that B and A are programmed directly in the N register**

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To program in a value for the N counter, the A counter, B counter, and prescalers are specified, which specifies N. Note from the proceeding slide that B>=A. This must be checked for each value of N programmed into the chip. A prescaler must be chosen before these calculations are used. e.g. for a 64/65 prescaler, P = 64

Recall:

equation 1: $N = P*B + A$

to determine B, apply the div operation (also called "trunc" which means divide and disregard the remainder) to both sides of the equation to yield:

$N \text{ div } P = (P*B + A) \text{ div } P = P*B \text{ div } P + A \text{ div } P = B$

(recall that A div P = 0 since A< P)

B = N div P

Once B is known, A can be determined algebraically, or by applying the mod operation (short for "modulo", which means disregard the quotient and take only the remainder)

$N \bmod P = (P*B+A) \bmod P = P*B \bmod P + A \bmod P = A \bmod P$

A = N mod P

The minimum continuous divide ratio is a sufficient condition, but not a necessary condition. In other words, there are a few isolated cases where N< P*(P-1), yet the prescaler is still usable.

If **N>= P*(P-1)**, then **B>=P-1**. However, since A<P, this guarantees **B>=A**. This is convenient in checking a range of N values.

Dual Modulus Prescaler Example

- **Assume the Following:**
  - **Fout = 1000 MHz**
  - **Fosc = 10 MHz**
  - **Fcomp (channel spacing) = 100 KHz**
  - **P = 128**
- **Determine Counter Values**
  - **R = Fosc / Fcomp = 10 MHz / 100 KHz = 100**
  - **N = Fout / Fcomp = 1000 MHz / 100 KHz = 10000**
  - **B = N div P = 10000 div 128 = TRUNC(78.13) = 78**
  - **A = N - (B • P) = 10000 mod 128 = 16**

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Note that is is first necessary to select a prescaler to use. In this case, a 128/129 prescaler is used. If the initial selection of prescaler does not work, they try a different prescaler. The available prescalers are specified in the selection guide and the data book. After the prescaler is chosen, it is essential to confirm that B>= A for that particular value of N for proper operation.

For this particular example, the minimum continuous divide ratio is 128*(128-1) = 16256. Since 16256 is greater than N = 10000, we can not conclude yet that this is a legal N value, and it is necessary to check B>=A. Had N been greater than 16256, the work would have been done. Here is a summary of some of the other N values.

N	B	A	Legal Divide Ratio?
10000	78	16	yes
10001	78	17	yes
. . .			
10062	78	78	yes
10063	78	79	no
…			
10111	78	127	no
10112	79	0	yes
...			

Sufficient Prescaler Conditions

(If these conditions are met, then the necessary conditions will also be met. Note that this assumes an 11 bit B counter.)

Prescaler	Min. N (Continuous)	Max. N
8/3	56	16383
16/17	240	32767
32/33	992	65535
64/65	4032	131071
128/129	16256	262143
P/(P+1)	P•(P-1)	2047•P+P-1

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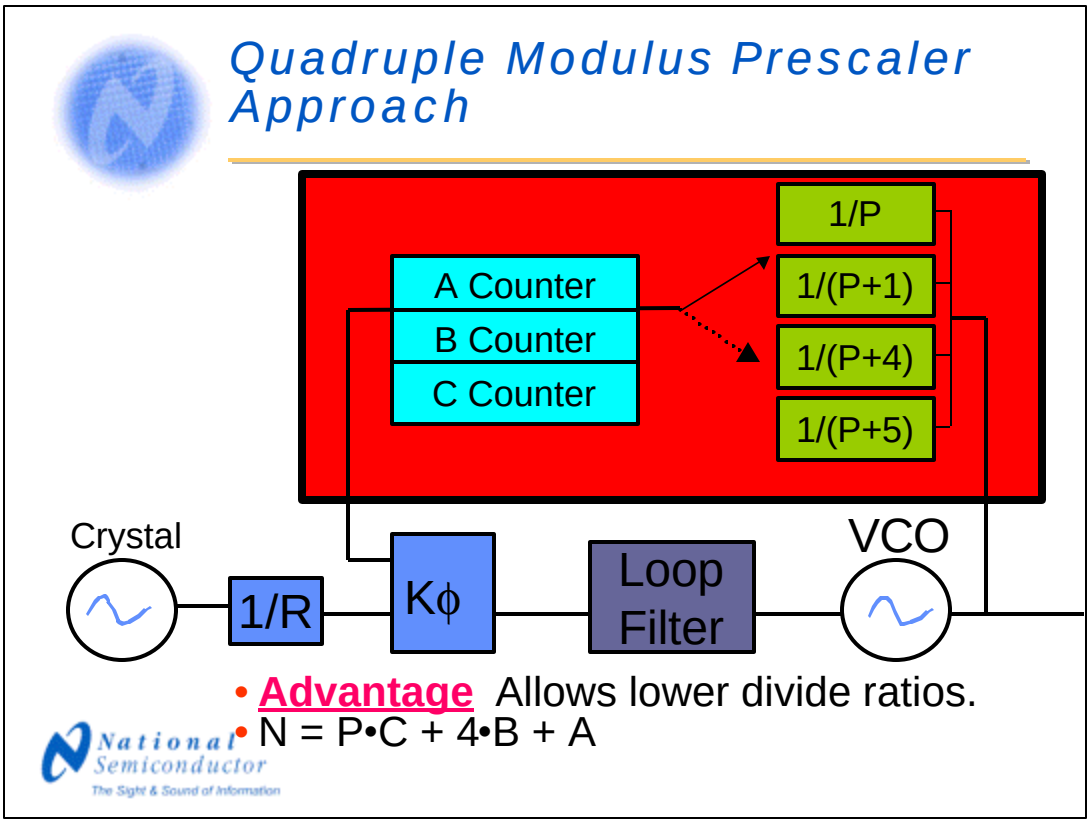
This chart is included for reference.

The minimum N value is the minimum continuous divide ratio for the given prescaler. Note that smaller prescalers have lower minimum continuous divide ratios.

The maximum value of N is limited by the fact that the B counter has a finite number of bits. In this case, it is assumed that the B counter has 11 bits. This is true of the majority of National's PLLs.

This chart can be used to help determine which prescaler can be used. If the desired value of N is below the minimum N listed, it still may be achievable, and the only way to know is to check B>=A. Note that this assumes an 11-Bit B counter. Some parts have a different size B counter.

Also be aware that for the lmx2350/52 only, these parts have the requirement B>=A+2. This rule only applies to these 2 parts.



Quadruple Modulus Prescaler Operation

The quadruple modulus prescaler works by having four possible values to use as a prescaler, although only three are used for any given N value.

Solving for C, B, and A

A greatly simplifying assumption is that P is a multiple of 4. Practically, this turns out to be true just about all the time. Assuming this, we get:

C = N div P

A = N mod 4

B = (N – P*C)/4

Note that C>=max{A,B} for proper operation

Note that A<4 and B<P/4 are restrictions for A and B as well.

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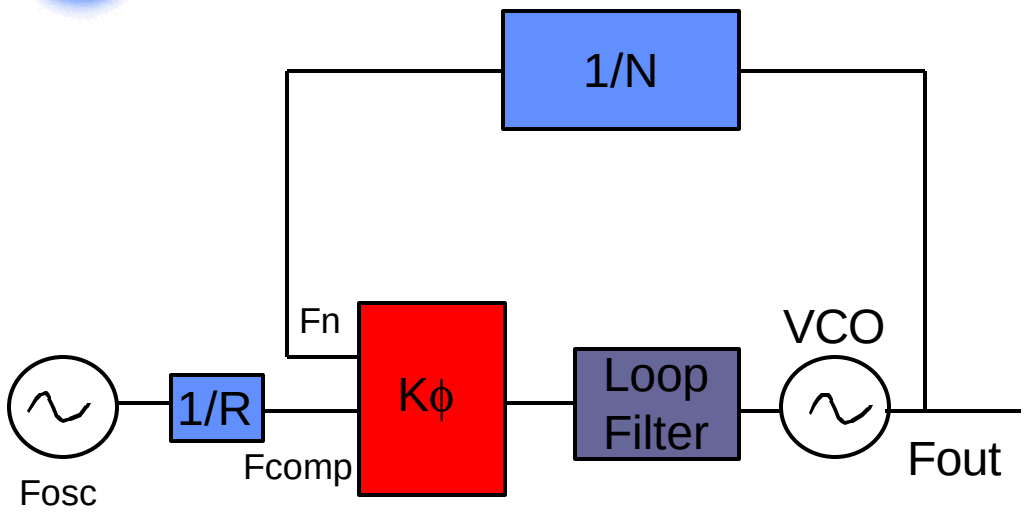
Phase Frequency Detector/Charge Pump



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Phase/Frequency Detector (PFD)

- **Detects differences in input signals**
  - **Detects phase error between 2 input signals**
  - **Detects frequency error between 2 input signals**
- **Outputs a voltage to the charge pump**
  - **The average value of this voltage is proportional to the phase/frequency error.**
    - **It is actually a fixed voltage amplitude with a variable duty cycle.**
  - **Along with the rest of the system, ensures the 2 input signals are the same frequency and phase**
- **Usually the charge pump and PFD are integrated together**

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The phase - frequency detector is integrated with the charge pump. On some PLLs, the outputs ϕr and ϕp are given so that an external charge pump can be used.

Charge Pump Highlights

- **Charge Pump/Phase-Frequency Detector**
  - **Sources Current if output frequency/phase is too low**
  - **Sinks Current if output frequency/phase is too high**
  - **High Impedance (tri-state)if output frequency/phase is correct (within tolerances)**
- **Charge Pump Figures of merit**
  - **Want source and sink currents closely equal**
  - **Want tri-state to be very low leakage current**

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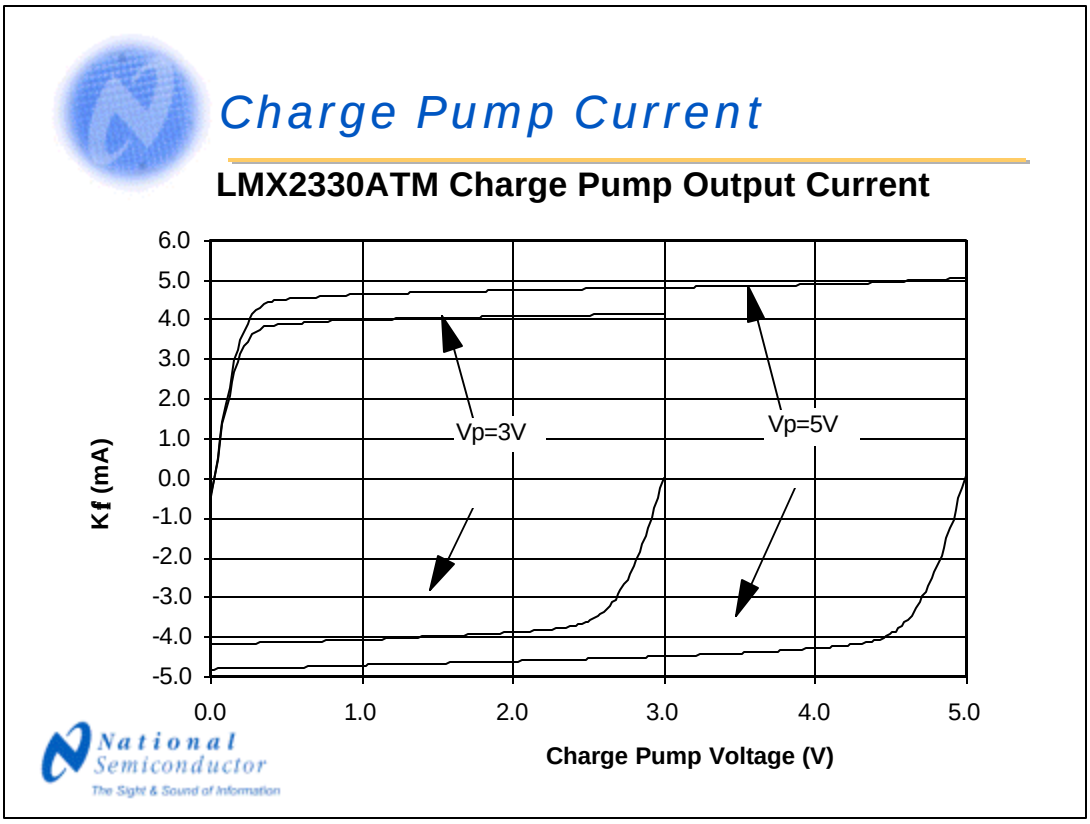
In the PLL, the comparison frequency is compared with the frequency obtained by dividing Fout/N, often denoted fp. If these 2 frequencies are the same, then the PLL is considered to be in lock and theoretically, the output of the charge pump should be 0 (high impedance state). In practice there are alternating positive and negative pulses of current with a period equal to the reference period, and these pulses are about 20-50 nS wide.

When out of lock, either positive or negative pulses are given to adjust the voltage on the loop filter, which adjusts the output frequency. For instance, when the output frequency is too low, there are positive pulses pulses of current, the width of these pulses increases with the amount that the PLL is out of lock, which increase the VCO voltage, which increase the output frequency.

Theoretically, the charge pump should sink and source the same amount of current, but in practice, there will always be some degree of mismatch. This mismatch can cause reference spurs and effect lock time, and is undesirable.

National specifies a typical and maximum mismatch in the databook. The charge pump current can also vary with the voltage on the loop filter, and over temperature.



The charge pump has 3 states:

1. Sink Current
2. Source Current
3. Tri-state (High Impedance)

This slide shows that the amount of current sunk and sourced changes with the supply voltage and with the charge pump voltage (which is equal to the tuning voltage to the VCO). Inferences about charge pump mismatch and variation can be made from this slide. Typically, the charge pump is not operated " Near the Rails", since the graph looks very nonlinear in this region. Note that these curves are inverted. The reason for the inversion is the way that National tests charge pump currents.

Charge Pump Mismatch

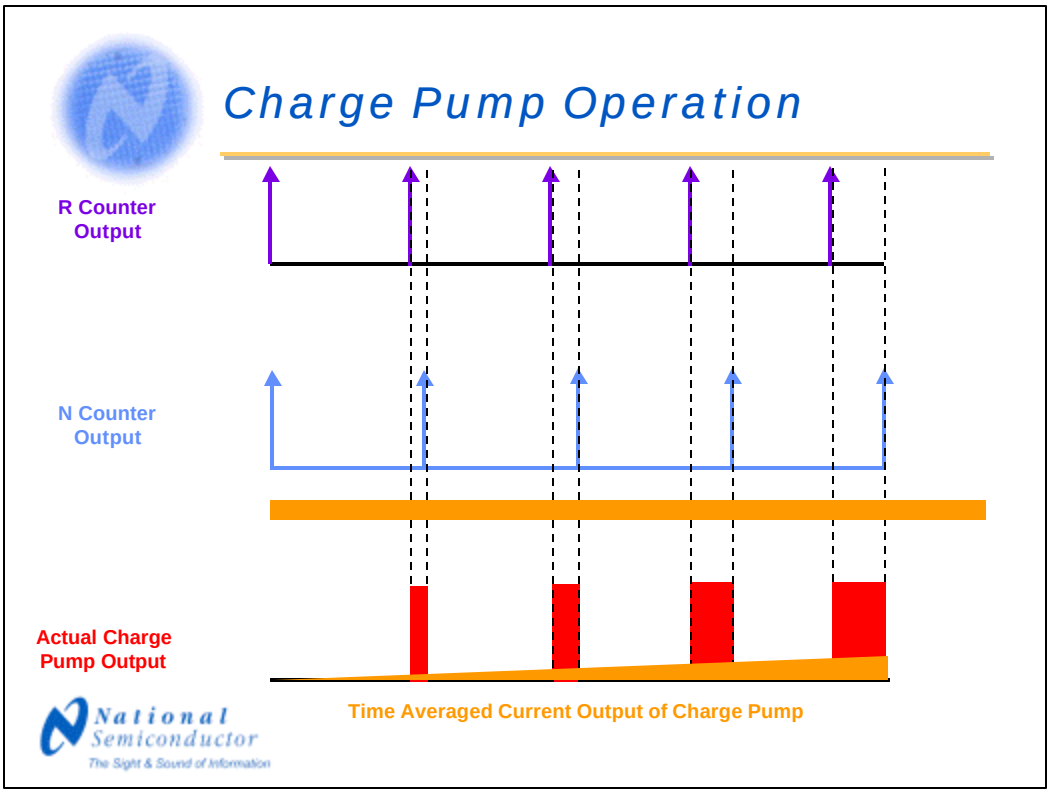
Charge pump mismatch is a measure of how well the sink and the source currents are matched. 0% mismatch is theoretically the most desirable, but sometimes a slight positive mismatch is desirable because the turn on time of the source transistor is slower than the turn on time of the sink transistor.

Charge Pump Balance

Balance describes how constant the charge pump currents over the charge pump voltage. A perfectly balanced charge pump would put out the exact same amount of current regardless of the charge pump voltage.

Charge Pump Leakage

Actually, the graph on this slide has nothing to do with charge pump leakage, although this is also an important parameter. In the locked state, the charge pump is off for most of the time. When the charge pump is off, the current should be 0 mA, but in fact there is a very slight current (usually in the nA range) when the charge pump current is off.



Charge Pump Operation

The charge pump puts out a pulse width modulated signal. It can source current, sink current, or be high impedance. Whenever the R counter has a positive transition, there is a positive transition for the charge pump output. That means if it was sinking current, it is tri-state. If it was tri-state, it sources current. If it was already sourcing current, it continues to source current. Whenever the N divider has a positive transition, the charge pump has a negative transition. This means that if the charge pump was sourcing current, it becomes tri-state. If it was tri-state, it sinks current. If it was already sinking current, it continues to sink current.

Continuous Time Approximation

For the sake of simplicity, it is usually fair to model the charge pump current as an analog current which has a value equal to the time-averaged value. This value is shown with the orange curve. This approximation is the continuous time approximation and is valid provided that the sample rate is sufficiently high relative to the bandwidth of the loop filter. The loop bandwidth will be discussed in later sections.

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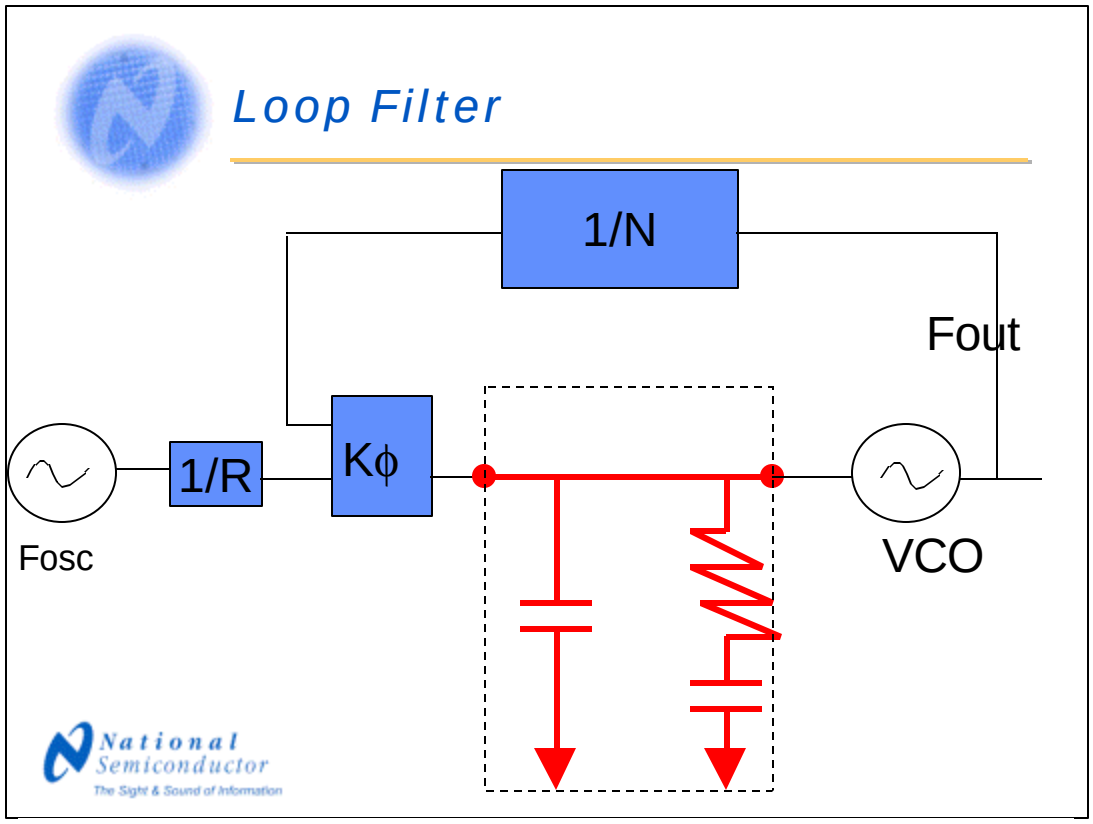
Loop Filter
1/N
Fout
1/R
Kϕ
Fosc
VCO
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Loop Filter

- The Loop Filter is a Low Pass Filter
  - It can also be thought of as an integrator with some added components
- The Loop Filter determines a lot about PLL performance
  - Switching Time
  - Loop Bandwidth (Related to RMS Error)
  - Reference Spurs
- The Loop Filter is external to the chip and is application specific
  - National Has Loop Filter Design Software at wireless.national.com (EasyPLL)

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